28.5 A 1ps-Resolution Jitter-Measurement Macro Using Interpolated Jitter Oversampling

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With the continued increases in chip performance that accompany device-process scaling, the inability to directly measure on-chip jitter has become a serious issue, and on-chip jitter measurement macros [1][2] appear to be an attractive solution. Our newly developed jitter measurement macro has three key features that help attain high-resolution real-time successive *in-field* jitter measurement: (a) a novel interpolated jitter oversampling technique that achieves 1ps measurement resolution, (b) a hierarchical vernier jitter measurement technique that does not need to use analog I/O ports for *in-field* measurements and exploits the trade-off between random jitter (Rj) and deterministic jitter (Dj) measurement characteristics, and (c) a feedforward calibration technique that improves the immunity to process variations while maintaining a small circuit area.

Figure 28.5.1 shows a timing diagram and a power spectrum for conventional jitter measurement. The timing difference between a reference clock (REF) and a measured clock (SIG) is observed every cycle, i.e., $\Delta t1$, $\Delta t2$, etc. Measured results are converted to quantized digital data, and the resulting quantization error may be expressed as a noise spectrum. The bandwidth of the noise spectrum is half of the clock frequency, $f_0/2$, the same as the bandwidth of the jitter spectrum, which means that the noise spectrum cannot be reduced by low-pass filtering without attenuating the jitter spectrum. To improve resolution, we propose an oversampled jitter measurement. While noise intensity is strongly dependent on sampling frequency, this frequency, which is equal to the clock frequency, cannot generally be increased. To increase sampling frequency above that of the clock frequency, we have introduced phase interpolators which successively generate four sampling points per clock cycle, thus achieving a 4× sampling frequency. By extending the noise spectrum from $f_0/2$ to $2f_0$, this oversampled measurement makes it possible to suppress three-fourths of the quantization noise power. The high-frequency components of this noise can be attenuated by a digital low-pass filter.

In the jitter measurement macro (Fig. 28.5.2), 4 separate-phase clock signals for 4× oversampling are created in each of the two interpolation blocks. Each of these can be fed to one of the four small measurement-range jitter measurement macros, referred to here as micro-measurement macros (μMs).

Figure 28.5.3 shows a conventional high-resolution jitter measurement macro; a vernier delay line [1] that contains series-connected vernier delay-cells in which the delay difference between individual delay lines is set to τ. It also contains comparators for measuring phase differences between vernier delay-cell input values. With this design, the phase differences between REF and SIG can be measured with a resolution of τ. Because the latency of the measurement macro increases at a rate proportional to the measurement range however, an increase in the range will result in an increase in internal jitter and will degrade the maximum operating frequency. A latency of 16 delay cells (16Ts), for example, would be required to support a measurement range of 0 to 15τ. To suppress the latency, we use hierarchical vernier clock delay lines. As REF and SIG propograte along the coarse delay lines, the phase difference between them decreases by 4τ at each vernier delay cell. These signals are then fed into fine delay lines in which the delay difference between individual delay lines is set at τ. This hierarchical structure is able to shorten latency from 16Ts to 4Ts because the propagation delay of each vernier delay cell in the coarse delay lines is the same as that in the fine delay lines.

In order to control the relative oversampling rates and jitter-measurement ranges, we use the modes shown in Fig. 28.5.4. In the 4× oversampling mode, in which signals are input to μMs from 4 separate phase clocks, the jitter-measurement range is the same as that of a μM, but three-fourths of the quantization noise intensity is suppressed. In the 1× oversampling mode, the phase difference between signals output from μM1 is 16τ smaller than the phase difference between REF_0 and SIG_0 (see Fig. 28.5.3). In μM2, it is possible to measure the phase difference between REF_0 and SIG_0 within the range of 16τ to 31τ by inputting to μM2 the output signals from μM1. Thus, the measurement range of 4 serially-connected μMs is 4 times larger than that of single μM. The 4× oversampling mode is able to precisely measure the small Rj. By way of contrast, the 1× oversampling mode is used to perform on-chip measurements over a wider jitter range in order to locate trouble spots in clock distribution networks.

Device matching constraints play a considerable role in determining the accuracy and performance of the measurement macro. The main sources of phase spacing variation in μMs are (1) delay variation in vernier delay cells and (2) comparator offset voltage variations that appear as effective phase errors. Conventional offset calibration procedures are mainly based on statistical analysis [2], but this approach requires a complex algorithm. In our simpler calibration procedure (Fig. 28.5.5), in order to detect the offset of delay cells and comparators, (a) the same signal is applied to two input nodes of a μM, and (b) the latencies of both delay lines in each vernier delay cell are set to Ts. In this setting, the timing difference between two signals input to the comparator should be zero. First, the C_0 offset is compensated for by selecting offset modulation signals for which the probabilities of C_0's output being 0 or 1 are the same. Next, the C_1 offset and delay line variations in D_1 are compensated for on the basis of monitoring the C_1 output. After C_1 and D_1 are calibrated, no recalibration of C_0 is required because the modulation results for C_1 and D_1 do not influence the C_0 offset. In this way, calibration can be completed without any need to recalibrate previously compensated comparators and delay lines. Here, a measured maximum phase spacing error before calibration of 5.3ps was successfully reduced to 1.4ps.

In order to avoid the large area overhead that results from storing calibration data in flip-flops, we use a compact calibration data input circuit which provides a 7b latch cell and a 1b flip-flop to each comparator and delay cell set. Flip-flops change active latch cell lines sequentially. This design requires only half the area of the conventional flip-flop array.

With conventional offset-tunable comparators [2], a special external design is required for distributing precharge clock signals to individual comparators. This is unnecessary with our comparators because each comparator precharges itself; the precharge clock signals are generated on the basis of the two input signals. When both inputs are low, the precharge signal PC also goes low and the output nodes S and SB will be precharged.

A micrograph of the macro, fabricated in a 90nm ASPLA CMOS process, is shown in Fig. 28.5.6. The area is 712μm×340μm.

In Fig. 28.5.7(a), Rj measurement results for on-chip jitter measurement macros are compared to real-time oscilloscope results. In the 1× oversampling mode, quantization noise is sharply defined and the measured peak-to-peak jitter (18.8ps) and the RMS jitter (2.64ps) are larger than the oscilloscope results by 5.8ps and 0.61ps respectively. By way of contrast, in the 4× oversampling mode, this difference is less than 1ps for each. Figure. 28.5.7(b) illustrates large Dj measurement results. Here, where timing jitter is larger than the measurment range of a μM (15τ), and the 4× oversampling mode cannot be used, the lower precision of the 1×-oversampled mode is far less significant, and the results are sufficiently meaningful.

References:
[1] N. Abaskharoun et al., “Circuits for On-Chip Sub-Nanosecond Signal Capture and Characterization,” *IEEE Proc. CICC*, 2001.
[2] D. Weinlader et al., “An Eight Channel 36Gsample/s CMOS Timing Analyzer,” *IEEE ISSCC Dig. Tech. Papers,* pp. 170-171, Feb., 2000.

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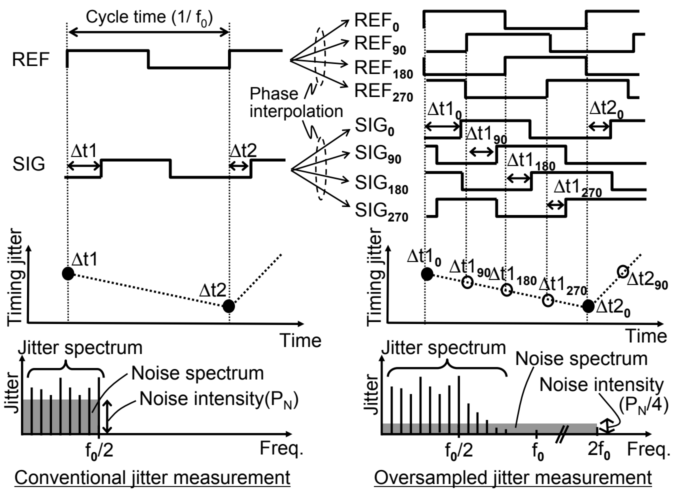


Figure 28.5.1: Interpolated jitter oversampling.

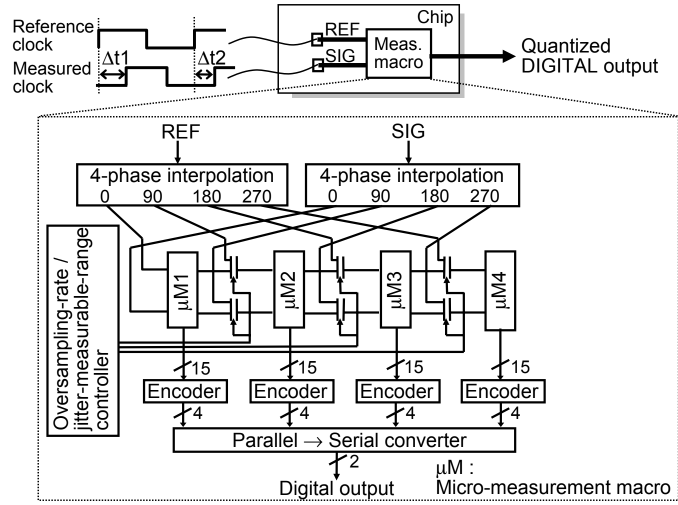


Figure 28.5.2: Jitter measurement macro with 4μMs.

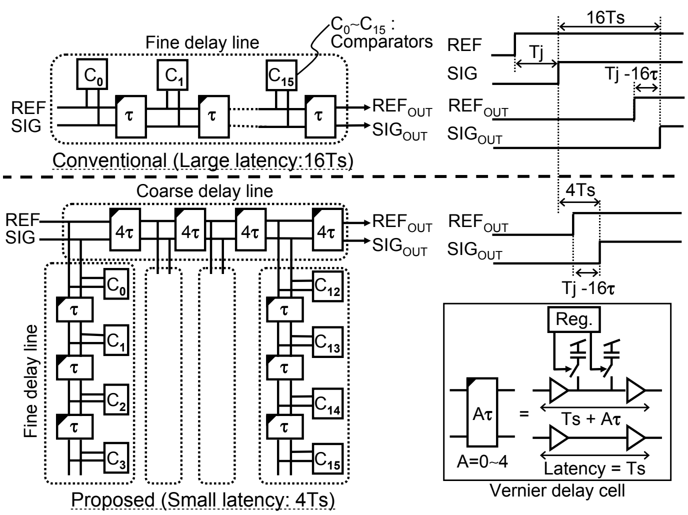


Figure 28.5.3: μM with hierarchical vernier delay line.

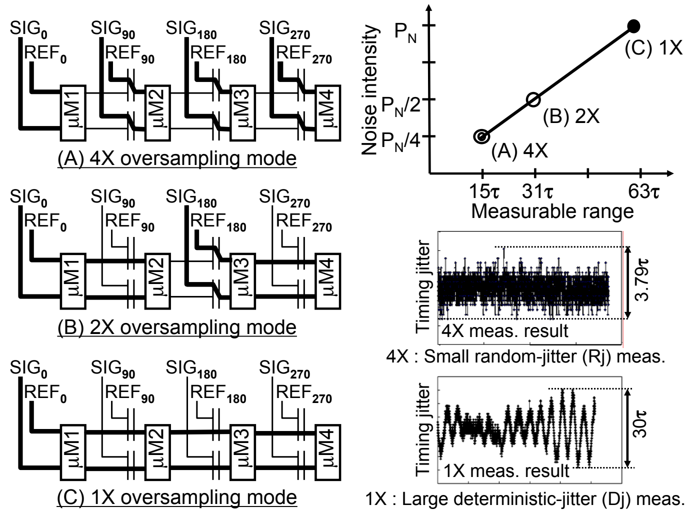


Figure 28.5.4: Oversampling rate and jitter measurement range control.

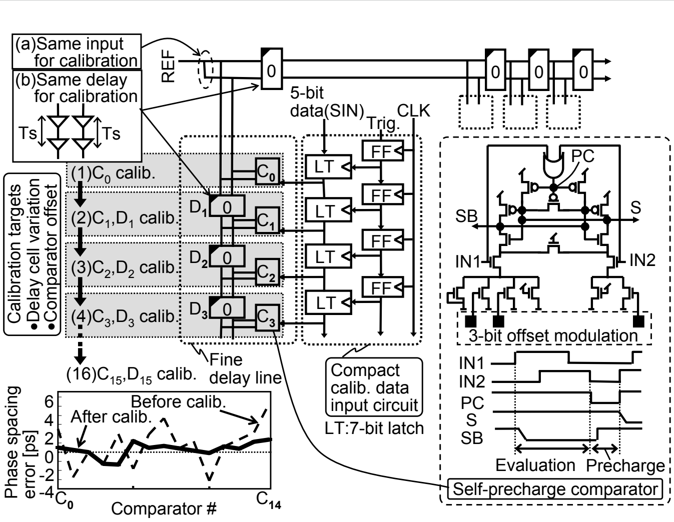
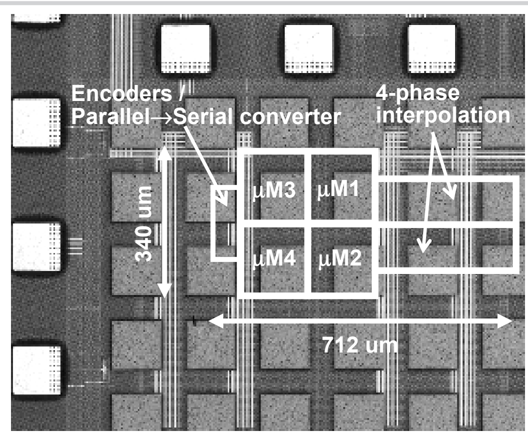


Figure 28.5.5: Feed forward calibration technique for μM.



Process	90nm CMOS
Supply voltage	1.0V
Metal	6-layer

Figure 28.5.6: Chip micrograph and process features.

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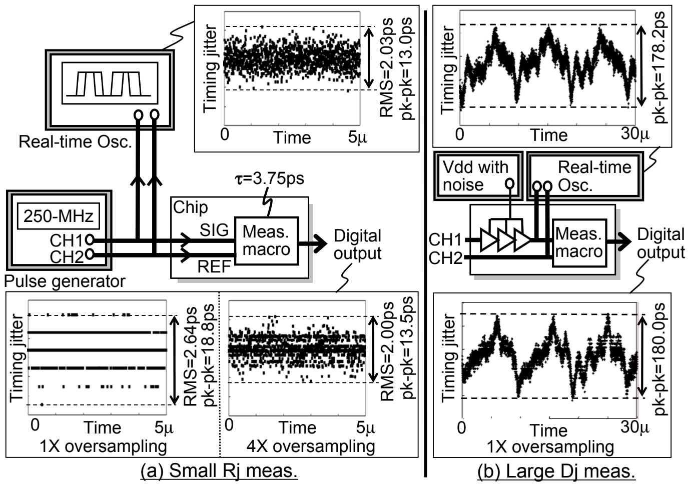

Figure 28.5.7: Measured jitter.